PRESETTABLE ANALOG INTEGRATOR

The basic analog integrator can be easily reset to zero using a field-effect transistor. Its offset, when reset, and its drift can also be easily nulled by shorting the integrating capacitor. However, a simple integrator does not offer means of presetting it to a desired initial value. Latching can be done by disconnecting its input, but there will always be some drift due to the input current of the operational amplifier and possibly also some droop due to the leakage of the integrating capacitor.

This paper describes a low-speed precision analog integrator that is used in the PID temperature controller of our **AVS-48SI Picobridge** (a cryogenic resistance bridge). The integrator consists of two op amps, a cheap analog multiplexer plus some other components. An external voltage from a source like a digital-to-analog converter can set the initial voltage from which integration begins. The integrator can also be latched to a preset voltage for any length of time without drift.

Figure 1a shows the normal condition, when the circuit (U2) is integrating V_{IN}. U1 is not used, it has been connected as a voltage follower in order to be stable.

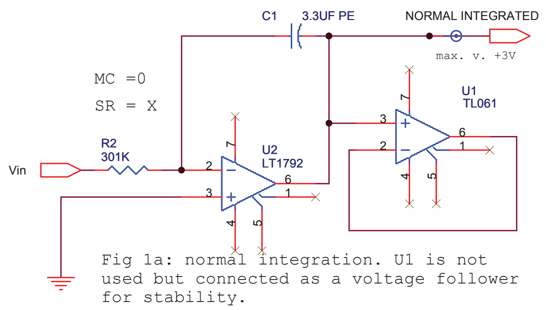

Fig 1a: normal integration. U1 is not used but connected as a voltage follower for stability.

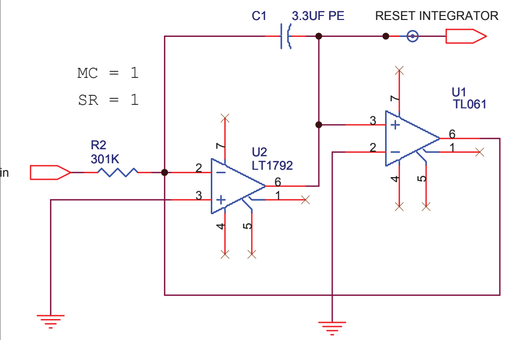

Fig 1b: Integrator is reset by grounding the inv. input of U1. U2 provides the required high-gain negative feedback, which tries to keep 3/U1 at zero. C1 limits high-frequency gain ensuring stability.

Figure 1b is the reset condition. U1 is now used as a comparator, that compares the output of U2 with zero. Comparator output is integrated by U2, which limits the bandwidth and provides the required negative feedback. Because of the low output impedance of U1 and high R2, there is no need to disconnect the input during reset or preset.

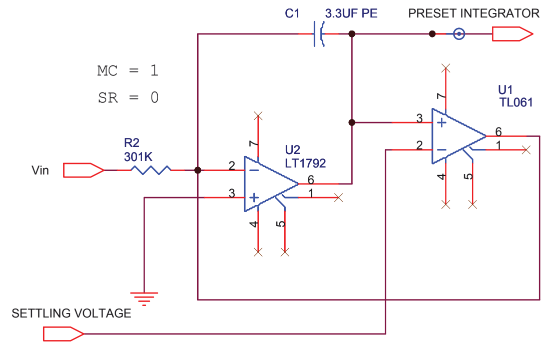

Fig 1c: Instead of grounding the inverting input of U1, it is connected to a source, like a DAC, that provides the settling voltage.

Figure 1c is the preset condition. It is exactly similar as when resetting, except that input to U1 is the preset voltage instead of zero. If the preset voltage can go to exact zero, then this mode is sufficient without need to change mode for resetting. A separate reset mode has, however, the benefit that there is no need to change the preset voltage just for resetting.

The complete schematic on the next page shows the two trimmers for drift and offset (P1 and P2). Selection of U2 is based on its low drift, voltage noise and input current. U1 has low voltage drift. Both have FET inputs and are specified for ±5V supply operation. Resetting is made by Q1, which needs a gate voltage more negative than -5V in order to be properly off during integration. Components that affect stability during reset and preset (R5, R7, C2, C3) were suitable for these opamp types, but if other circuits are used, different values may need to be found. This circuit is used for very long integration times, which explains the 3.3µF value of C1 and large value of R2.

The oscilloscope photo shows settling from 0 to 2.99V. Because of the ±5V supplies, our circuit is limited to 3V maximum output.

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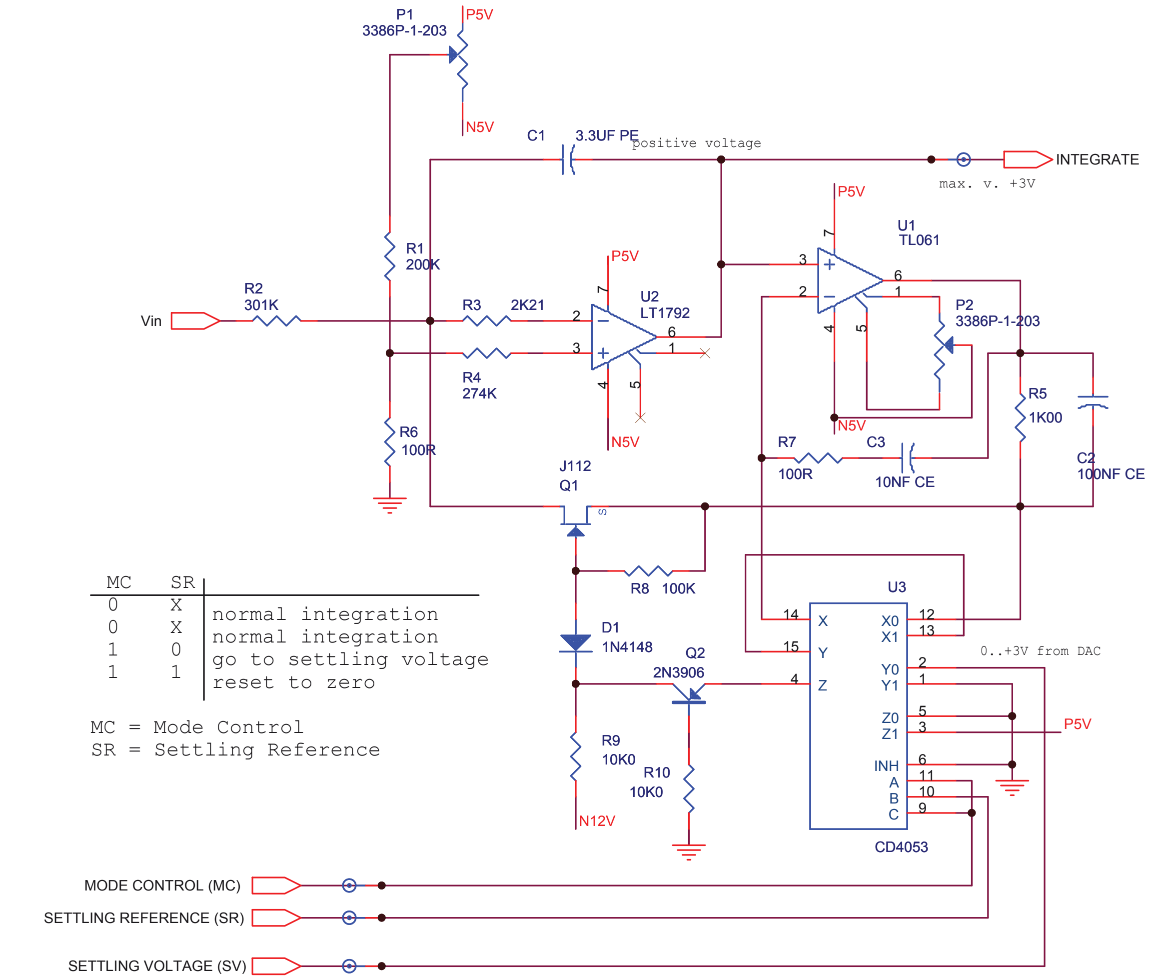
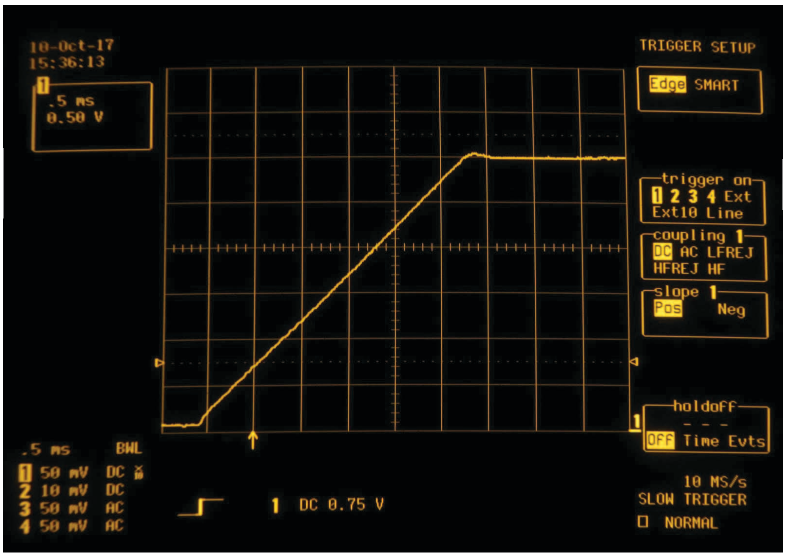


Fig 2: Complete schematic of the presettable integrator



This low-speed integrator slews from 0 to 3V in about 3 milliseconds. A smaller C1 makes slewing faster.