BIPOLAR CURRENT SOURCE CAN BE TRIMMED FOR OFFSET, GAIN AND R_{OUT}

We were looking for a bipolar current source that could be trimmed for zero offset, gain and high output impedance. Such a source was needed for very a low current DC application in the range of microamperes. After having compared some alternatives, we designed a little different schematic that required a little more components, but provided some extra advantages.

The simplest circuit

Figure 1a shows the simplest possible bipolar current source. It was out of consideration, as it requires a floating load, whereas our load was grounded. Its main virtue is its high input impedance, which does not load the driving source.

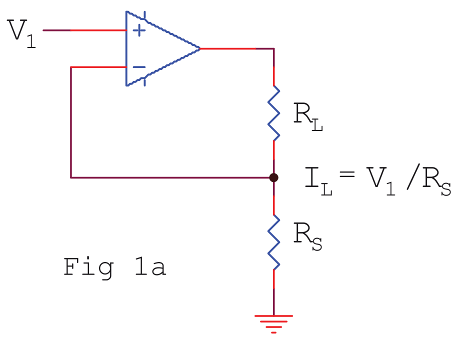

Fig 1a

The Howland circuit

Figure 1b is the well-known Howland current source. In this basic form, it requires tightly matched resistor ratios so that $R_2/R_1 = R_4/R_3$ for high output imperance. Fortunately, one can replace any of the resistors by a resistor+trimmer combination for adjusting the ratios to be the same. If only one-ended input is required, the other input can be connected to an adjustable offset voltage source for nulling the zero offset. However, there is no way to obtain gains other than 1 . Output current is $(V_2-V_1)/R_3$ and it cannot be adjusted. Impedance of the driving source should be low – at least is must not change.

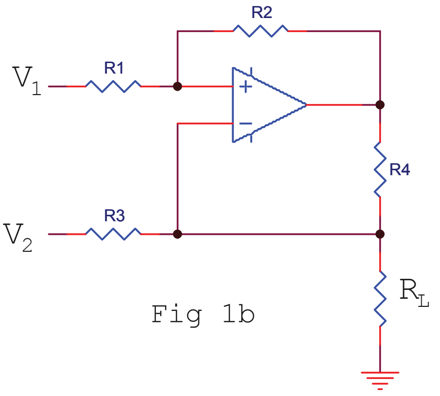

Fig 1b

Howland circuit for many output ranges

Figure 1c shows a Howland current source modified for easily changeable current ranges. Because of the added voltage follower, resistor R_5 determines the gain and it can be changed without effect to the output impedance. Exact trimming of course requires a resistor+trimmer combination. Offset and matching of R_2/R_1 and R_4/R_3 can be made as with the basic Howland circuit. This modified circuit is presented at least in AN-1515 from Texas Instruments. We found two drawbacks: If the ranges vary by decades, also the adjustment trimmer must be changed. At the cost of adding a third buffering opamp either before V_1 or V_2, one can eliminate the effects of loading a non-zero impedance signal source.

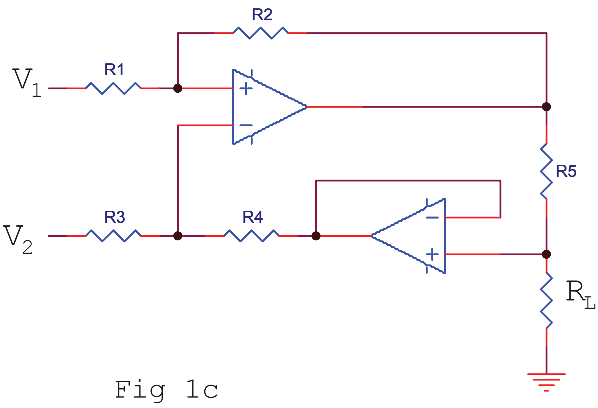

Fig 1c

Our design

Figure 1d shows our design without any extras. The principle is simple: Feedback is obtained by using the high-Z inputs of a 3-IC differential amplifier to sense the voltage drop across the shunt resistor R_S.

The desired value for this drop is fed in differential form to the ends of the gain-determining resistor R_3. The circuit tries to make these two effects equal, and the success is the better the higher is the gain of the U_1C-stage. The output current becomes independent of the load resistance R_L.

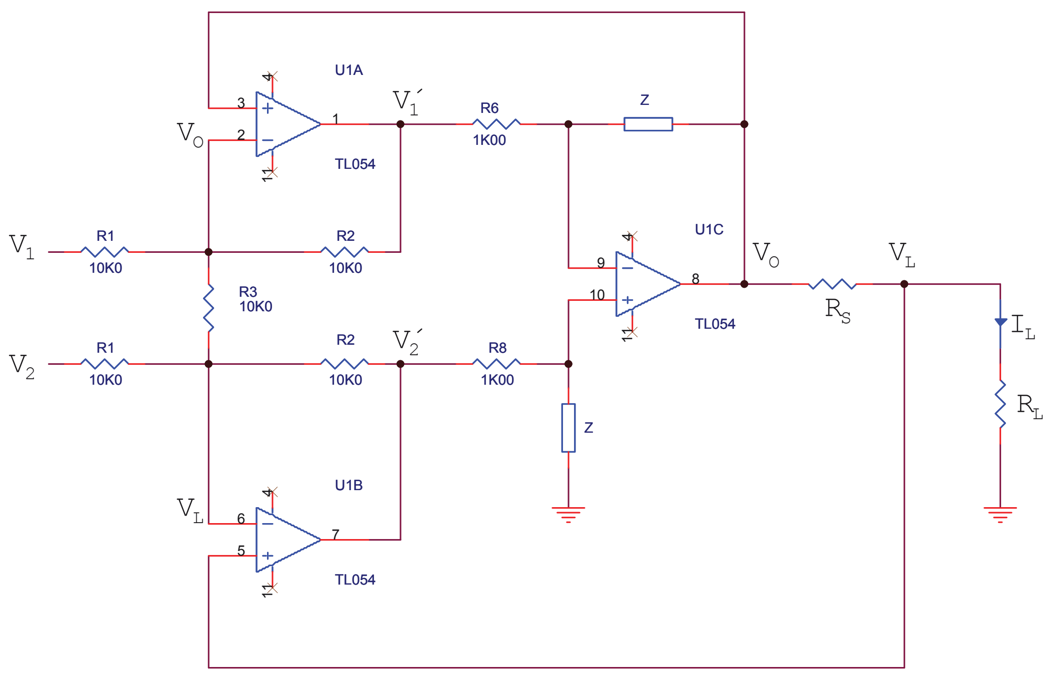

Fig 1d

Calculation is a bit lengthy even for the above case, where we have already used same values for R_1 , R_2 and R_3 for simplicity.

Currents into the inverting inputs of U1A and U1B must be zero:

$$\begin{cases} \dfrac{V_1 - V_O}{R_1} + \dfrac{V_L - V_O}{R_3} + \dfrac{V_1' - V_O}{R_2} = 0 \\ \dfrac{V_2 - V_L}{R_1} + \dfrac{V_O - V_L}{R_3} + \dfrac{V_2' - V_L}{R_2} = 0 \end{cases}$$

Solving for the differential output of the first stage:

$$V_1' - V_2' = (1 + 2\frac{R_2}{R_3} + \frac{R_2}{R_3})(V_O - V_L) - \frac{R_2}{R_1}(V_1 - V_2)$$

For this case, we are assuming that $R_1 = R_2 = R_3$ so that

$$V_1' - V_2' = 4\,(V_O - V_L) - (V_1 - V_2)$$

V_O is the output of the second differential stage

$$V_O = (V_1' - V_2')\,(-\frac{Z}{R}) \;\; ; \;\; (V_1' - V_2') = -\frac{V_O R}{Z}$$

where Z is some impedance. Further,

$$V_L = V_O \frac{R_L}{R_S + R_L} \quad ; \quad I_L = \frac{V_O}{R_S + R_L}$$

and subsituting

$$\left[4(1 - \frac{R_L}{R_S + R_L}) + \frac{R}{Z}\right] V_O = V_1 - V_2$$

Let now $Z \to \infty$, which means in practice that we replace Z by band-limiting capacitors in a DC or low-frequency application.

$$I_L = \frac{V_1 - V_2}{4R_S}$$

which shows that the load current is not dependent on R_L. There is, however, the scale factor 1/4.

If we do NOT set R3 = R2, the calculation goes as before, but the result is

$$I_L = \frac{V_1 - V_2}{C \bullet R_S} \quad \text{where } C = 2(1 + \frac{R_2}{R_3})$$

So the maximum gain that can be achieved by adjusting R_3 is 1/2. If a higher gain is needed, it must be accomplished by selecting a smaller R_S.

A practical circuit

The circuit of Fig 2 has trimmers for offset, output impedance and gain 1/Ci, which is set to 1/3. The buffer U1D is inverting and connected to the negative input. This is because we did not need high input impedance but we needed a circuit that does not deliver any arbitrary current if the input is left open.

The circuit is tuned as follows: With the input at zero, output of U1C is adjusted to zero using the offset trimmer. Then an external, high input impedance DVM is connected across R_S and the input is switched between two largely different values. P1 is adjusted iteratively so that the DVM display does not change. Finally, the gain is adjusted by applying

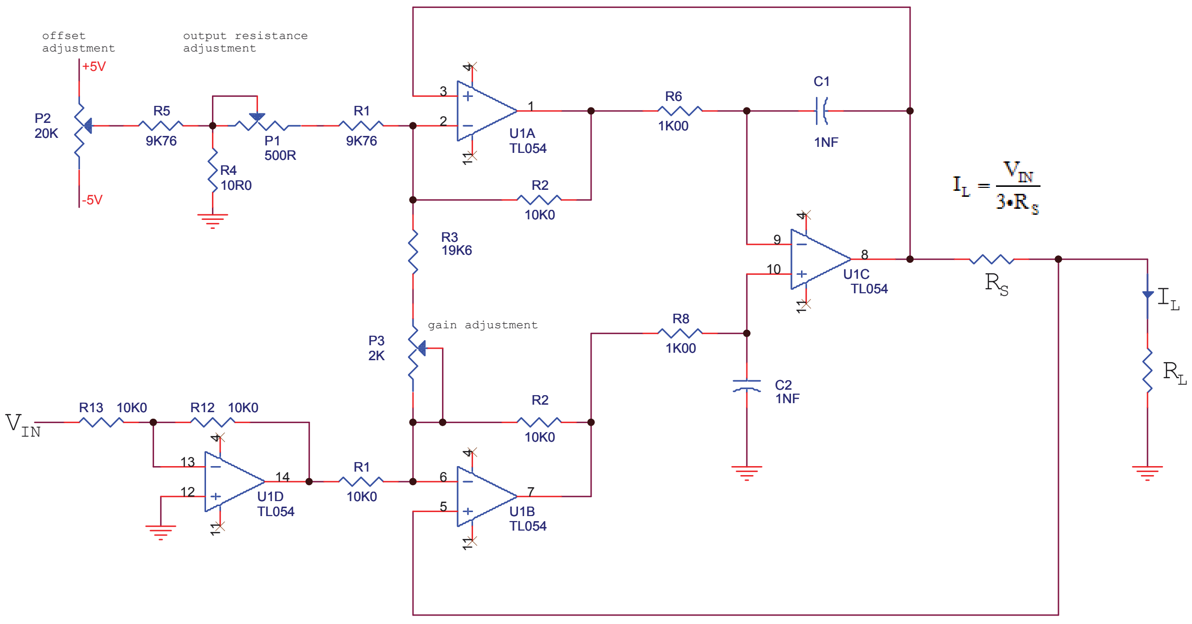

Fig 2

a known V_{IN} and measuring the voltage across R_S. This phase is sensitive to DVM's loading if R_S is high. In our case, R_S is 1MΩ and the current delivered when V_{IN}=3V is 1µA. Of course, the output current can also be measured with a precision current meter, if a suitable one is available.

Note that P3 can adjust the gain into both directions, whereas a series trimmer added to R_S could adjust gain only into one direction.

RV-Elektroniikka Oy Picowatt
Veromiehentie 14
01510 VANTAA, Finland

e-mail: reijo.voutilainen@picowatt.fi
Internet: www.picowatt.fi