

## AVS-48SI BLOCK DIAGRAM

The purpose of the large analog section of the AVS-48SI is to produce an output voltage, which is accurately proportional to the measured sensor resistance. This voltage is then subject to analog-to-digital conversion, but it can also be used for the 48's stepless analog temperature control or for driving the user's own temperature control system. Some, more digitally oriented resistance bridges, produce an accurate digital output but only a roughly calibrated analog output.

A low-frequency bipolar square-wave excitation current is fed through two series-connected resistors. The first is called injection resistor  $R_1$  (in our earlier bridges it was called "reference"), and the second is the unknown  $R_x$ . If the AC voltage drops across these two resistors are  $V_1$  and  $V_x$ , then  $R_x = R_1 (V_x/V_1)$ . Division of two analog voltages would be a very inaccurate operation, and therefore  $V_1$  is adjusted to a known constant value by means of feedback. The key part of the feedback loop is the null-indicating preamplifier, which compares the voltage drop  $V_1$  across  $R_1$  with a constant injection reference voltage  $V_{REF}$ . Both  $V_1$  and  $V_{REF}$  are symmetrical bipolar square waves in differential form. Negative feedback makes  $V_1 = V_{REF}$ . As  $V_1$  has now a known constant value, no division is required. Calibration of the AVS-48SI includes adjusting the magnitude of  $V_1$  for each possible combination of range and excitation. The output can also contain a zero offset, so that the equation becomes  $R_x = A + B * V_x * R_1$  where  $A$  is the offset and  $B$  is the gain calibration constant. Both  $A$  and  $B$  will depend on the combination of excitation and measuring range. A special automatic calibration process determines correct values for  $A$  and  $B$ , which are stored as an array in the non-volatile memory of the physically separate CPU unit. This array contains 128 elements. Whenever either range or excitation is changed, new calibration constants are taken from the array.

### Reference square

+3 Volts from a stable voltage reference is inverted and a symmetrical 12.5 – 13.64 – 15.0 Hz square (reference square) is formed. This is attenuated to a  $3\mu\text{V}..10\text{mV}$  level  $V_{REF}$ . Negative feedback will then

make the final excitation voltage  $V_1$  equal to  $V_{REF}$ . The attenuator has 8 steps in an approximate 1:3:3... sequence. Selection of the attenuation is controlled by the external CPU unit. The attenuated reference is fed to inputs C and D of the excitation channel preamplifier. Excitation current is the injection voltage  $V_1 (=V_{REF})$  divided by the injection resistance  $R_1$ . In order to generate a mismatch between the room-temperature injection resistor and the cooled sensor, the AVS-48SI tries to supply the required excitation current using as high injection resistance and as high injection voltage as possible. The mismatch between  $R_1$  and  $R_x$  reduces noise that the injection resistors can feed to the sensor. Another advantage is, that the larger is the injection resistance, the less sensitive the scale factor is to lead resistances.

### Excitation channel

The integrator of the excitation channel Phase Sensitive Detector (PSD) outputs some DC voltage. This voltage is inverted and chopped to a symmetrical square wave, which is then scaled down by the excitation channel attenuator. The attenuated voltage is connected to the "hot" end of the injection resistor  $R_1$ , which is selected by one of 7 reed relays on the preamplifier board. The resulting excitation current  $I_E$  is further directed by an 8-channel 4-wire multiplexer either to a sensor or to the selected calibrator.

The AC voltage drop across the injection resistor  $R_1$  is connected to inputs A and B of the excitation channel preamplifier. This specially designed preamplifier uses a dual-FET for comparing two differential voltages (A-B) and (C-D), where (C-D) is the differential reference voltage  $V_{REF}$ . The preamplifier produces null output if both *differences* are equal. As long as the two differences are unequal, the non-zero output from the preamplifier, which is further amplified by the variable-gain main amplifier, is subject to synchronous detection in the excitation channel PSD. The output from the PSD changes into proper direction, changing  $V_1$ , until the two differences are equal. Then the excitation channel outputs only random noise and a desired value for the excitation current  $I_E = V_1/R_1 = V_{REF}/R_1$  flows into the unknown resistance or into the selected calibrator resistor.

## Multiplexer

A maximum of seven sensors can be connected to the AVS-48SI. The sensor channels are wired to a female DC37 connector. Wiring is compatible with seven first channels of the older AVS-47B but numbering is different: The 8 channels of the AVS-47B are numbered 0..7, whereas the seven AVS-48SI sensor channels are numbered 1..7. Channel 0 is connected to calibrator references. The AVS-48SI uses DPST (double pole single throw) reed relays, so that 8 channels require 16 relays for 4-wire switching. In addition, selection of one of the 7 calibrators plus zero needs additional 8 relays. Three relays are required for programmable 4- or 2-wire configuration and for two alternative sensor grounding schemes. So there are 27 relays altogether on the multiplexer board. Signals that are multiplexed to the sensors are called:

- I+ excitation current out from the bridge
- V+ voltage at the “hot” end of the sensor
- V- voltage at the “ground” end of the sensor
- I- return of the excitation current

Usually cryogenic sensors have no connection to cryostat ground (“floating sensors”). With the AVS-48SI, any sensor’s I- lead can be connected to the cryostat (“grounded sensor”) as an alternative. Using a grounded sensor can improve its thermal contact or reduce required wiring or connector space. The bridge must be informed about such a change, there is a command for doing this.

## Calibrators

The AVS-48SI features seven wire-wound resistors with 0.1% initial tolerance. Their specified temperature stability is 3-5ppm/C and the expected long-term stability about 35ppm/year. These resistors are measured carefully at the factory before delivery, and their values are stored in a non-volatile memory of the CPU. Any one of these resistors, or zero resistance, can be selected programmatically. The so selected resistor is connected to multiplexer channel 0, and by selecting CH0, it can be measured like any actual external sensor. Calibrators can be used, in addition to facilitate the automatic self-calibration procedure, also for quality control by including one in a scanning sequence, for example.

## Signal channel

The purpose of the excitation channel was to adjust the excitation current to a well known constant value. The purpose of the signal channel is to measure the voltage drop across the unknown  $R_x$ . The two voltage leads from the sensor are connected, via the multiplexer, to inputs A’ and B’ of the signal channel preamplifier. The input stage compares voltage drop (A’-B’) with a differential feedback that is connected to inputs C’ and D’. Nonequality of the differences results in a signal at the bridge operating frequency. After much amplification, this signal drives the output of the signal channel phase-sensitive detector into a proper direction until the differences become equal. The output voltage is inverted and chopped into a symmetrical square. The square is attenuated by the same factor as the reference square  $V_{REF}$  and finally it is connected to inputs C’ and D’. Now the PSD output is directly proportional to the unknown resistance and it is the AVS-48SI’s primary output. But the output will contain zero offset and scale error, if these are not eliminated.

## Offset and scale

*Zero offset* is the output reading resulting from measurement of an exact zero resistance. We have not even attempted to realize a true zero resistance on the printed circuit board – it would be impossible. Instead, we take the advantage of the >100dB common-mode rejection ratio (CMRR) by wiring the V+ and V- inputs so that they are exactly at the same common mode potential which is as low as possible. Then the CMRR makes this connection behave like a very good zero resistance. Output of the signal channel PSD integrator output is adjusted to zero by adding a suitable voltage from a digital-to-analog converter to the feedback loop before chopping.

The magnitude of the required voltage is determined by the calibration procedure for each range/excitation combination.

*Scale error* is nulled by using another D/A converter to adjust the the +3V reference before it is chopped to reference square. The magnitude of the required voltage is determined by the calibration procedure for each range/excitation combination.

Note that both the offset and scale adjustments affect the analog output, which is actually the most accu-

rate output of the AVS-48SI. This analog output is then measured by the bridge's own A/D converter in order to make the digital output that can be sent to the external computer.

### Digital-to-analog converters

The AVS-48SI has one LTC2600 8-channel D/A-converter. Its outputs are used for

- correcting offset and scale factor errors ( 2 DACs) under firmware control. Required DAC voltages are determined by the calibration procedure.
- temperature control set point or setting null point for deviation display (1 DAC). User-controlled quantity.
- user programmable DAC (0.005V...2.99V) (1 DAC). This User-DAC is always available for the scientist's own purposes. It has a BNC output on the rear panel.
- direct control of the heater output (1 DAC). The heater can be turned into a software-controlled current source. It obeys the selected heater power range, but it is not dependent on the analog temperature controller. User can enter a voltage number from 0.005 to 2.99 V corresponding to almost zero to almost full range. This feature enables creating one's own digital control algorithms.
- The remaining 3 DACs are for presetting the two PSD integrators and the integrator in the PID temperature controller. Fast presetting of the phase sensitive detectors is currently not in use, whereas presetting the PID integrator prevents power jumps when the heater range is changed.

These DACs are not extremely accurate, and their performance must be improved in order to be compatible with the AVS-48SI's accuracy. This is accomplished by iterative feedback, which is best described by an example: Program commands a DAC to output 1.0000 volt. Because of its offset and scale errors, the DAC outputs e.g. 0.995 Volts. This voltage is measured by the very accurate A/D converter which reveals that the output was 0.005 V too low. The original command is now repeated, but with a new value of 1.005 Volts. This increases the output to exact 1 Volt. The advantage of this method is, that a cheap D/A converter can be made very accurate, but its disadvantage is the low speed. However, for

a low-speed instrument, like a cryogenic resistance bridge, this is acceptable.

### PSD synchronization

The crystal-controlled clock provides three alternatives for PSD operation, 12.5Hz, 13.64Hz and 15.0Hz. Changing the frequency has no visible effect on reading unless the signal from the sensor suffers from a mains-frequency interference. 12.5Hz should not be used in a 50Hz environment whereas 15.0Hz can be troublesome in a 60Hz country. If the interface has exact 50 or 60Hz frequency, the output will not beat when PSD operates at 50 or 60Hz, respectively, but there can be a constant offset shift, which is impossible to see. A small difference between PSD and interfering frequencies results in slow beating. This can be made faster and easier to suppress by filtering if another PSD frequency is selected. Because of these two reasons, choose the opposite frequency. Initial default is 13.64Hz, which guarantees good but not the best possible performance both in 50 and 60Hz countries.

It is also possible to override the internal clock by feeding an external 0/+5V square signal to the EXT CLOCK input. This allows even more freedom to change the PSD frequency.

### Digital outputs

The AVS-48SI communicates with the external world via Picowatt's own "Picobus" protocol. This protocol uses four wires to implement a synchronous, serial interface. Picobus is a slow, but almost bullet-proof protocol, whose greatest virtue is that it can be built using combinational and sequential logic circuits, without no digital intelligence. The fact that it does not need a microprocessor makes it very silent. This is important in cryophysics, where all RF leakages tends to heat the sensor, and therefore silent operation is our commitment. Operation of Picobus will be described in a separate article, but it should be considered a transparent connection between the analog bridge and the external CPU unit, which together make up the AVS-48SI.

In order to eliminate ground currents between the computer and the bridge, Picobus signals are optically isolated inside the bridge. However, the shielding braid must remain grounded in order to be a shield.



It is connected to the bridge enclosure (DE9P) but it is only capacitively connected to the CPU ground for high frequencies (DA15P). If only possible, the braid should be grounded to the conducting wall of the shielded cryostat room immediately at the entering point. If this is not possible, consider the optical link option.

### Analog outputs

The primary stepless analog output ranges from -3V to +3V. It is obtained from the signal-channel PSD integrator after filtering by a 3rd order analog Bessel filter. This filter removes most of the residues of the PSD frequency. The full +3V corresponds to full deflection on any selected measuring range. This analog output can be turned into deviation by a software command. The deviation is then  $|R_x - \text{set point}|$  whose polarity can be selected.

Control error is another stepless analog output. It has been taken before the analog filter in order to exclude the filter's delay from the closed PID control loop. A control loop can be made faster, if there are no unnecessary delays. The polarity command affects also the control error.

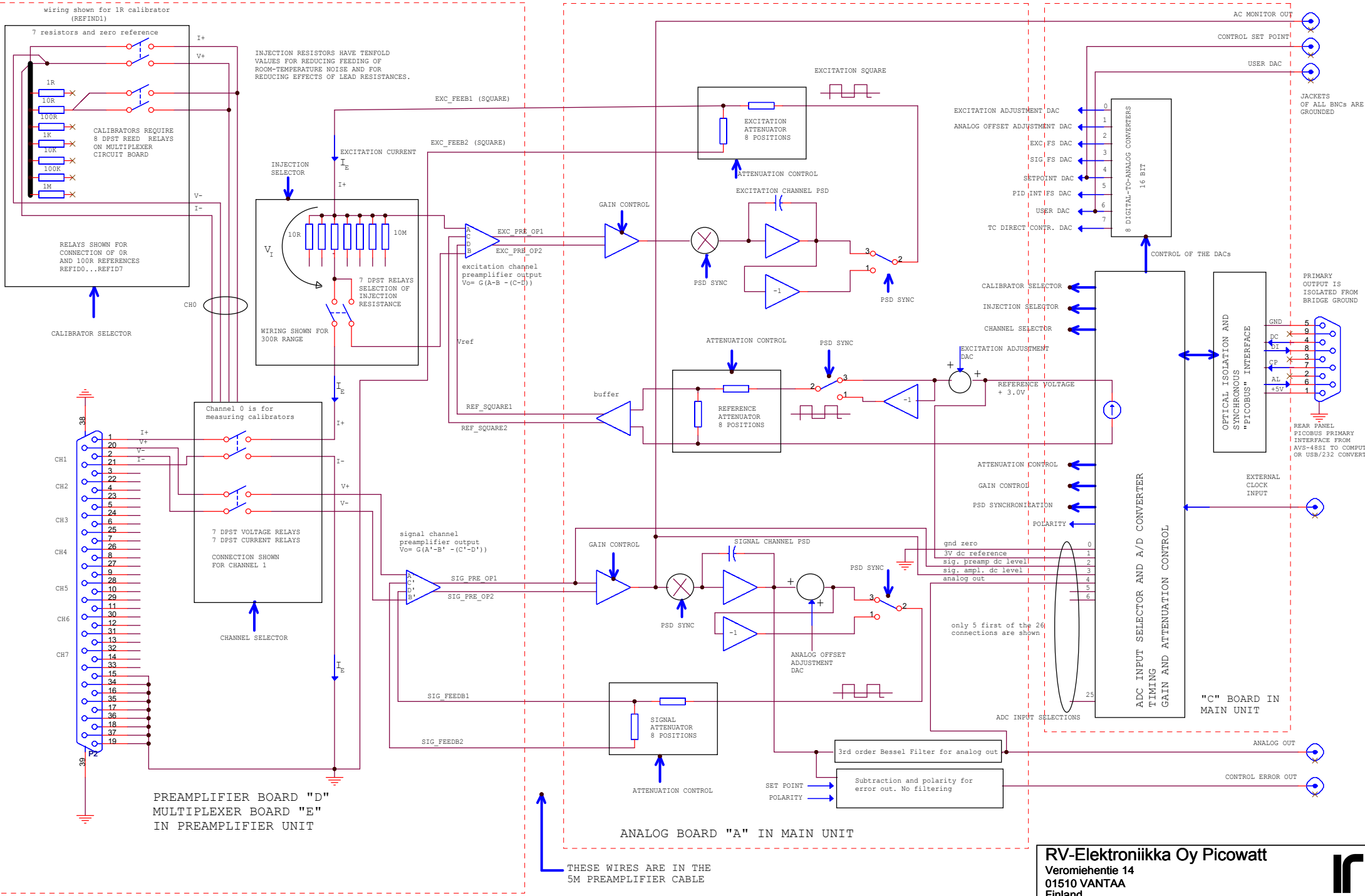
Some troubles can be viewed by connecting an oscilloscope to the AC Monitor Out BNC. It is the output of the signal-channel variable-gain amplifier. In an ideal case, the trace is smooth at least on lower ranges and high excitations. When excitation is reduced, the trace will show more and more random noise which comes from the preamplifier and/or sensor resistor. The scope shows clearly any possible mains hum or other unwanted interference. Some additional info about the interference may be got, if the scope has a fast FFT capability. Connecting the oscilloscope to the AVS-48SI is easy: the BNC connector has a grounded jacket. No differential, or floating, connection is required.

Two DAC voltages (0.005...2.99V) are also available. The User DAC is always available whereas the Control Set Point DAC is devoted to temperature control when control is active. If temperature control is not active, Control Set Point is available like the User DAC. The DACs do not tolerate much loading (see LTC2600 specifications from Linear Technology). If a more loadable output is required, or if the voltage levels or scaling must be changed, one can build a breadboard circuit and fix it inside the 48SI enclosure. The bridge has a -12/0/+12V

power supply for such a purpose.

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PREAMPLIFIER BOARD "D"  
MULTIPLEXER BOARD "E"  
IN PREAMPLIFIER UNIT

ANALOG BOARD "A" IN MAIN UNIT

"C" BOARD IN MAIN UNIT

THESE WIRES ARE IN THE  
5M PREAMPLIFIER CABLE

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